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10/530,848	05/06/2006	Armin Gerhard Aberle	85267	2457

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FITCH EVEN TABIN AND FLANNERY
120 SOUTH LA SALLE STREET
SUITE 1600
CHICAGO, IL 60603-3406

EXAMINER	
SLUTSKER, JULIA	
ART UNIT	PAPER NUMBER
2891	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/530,848	ABERLE ET AL.	
	Examiner	Art Unit	
	JULIA SLUTSKER	2891	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-90* is/are pending in the application.

4a) Of the above claim(s) *See Continuation Sheet* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4,6, 9-12, 21-25, 27,28,30,32-34,40,50,54* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *08/30/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Continuation of Disposition of Claims: Claims withdrawn from consideration are 2,3,5,7,8,13-20,24,26,29,31,35-39,41-49,51-53 and 55-90.

DETAILED ACTION

Claim Rejections - 35 U.S.C. § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 6, 9, 50, and 54 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 6, 9, 50, and 54 are unclear because they recite a verb tense form (e.g. "polycrystalline layer is doped") different from that used for claim limiting steps, which recitation therefore makes unclear whether this recitation is a limiting step or intended outcome.

Claim 54 is indefinite, since it is unclear when "completion of the cleaning step" occurs.

Correction is required.

35 U.S.C. § 112, first paragraph, requires the originally filed specification to contain a written description of the claimed invention. And 35 U.S.C. § 132(a) prohibits any "amendment [from] introduc[ing] new matter into the disclosure of the invention." Accordingly, new matter should not be introduced by either addition or deletion.

Claim Rejections - 35 U.S.C. § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to

a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1, 4, 6, 9-12, 21-23, 27, 28 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over "Surface morphology of poly-Si films made by aluminum-induced crystallization on glass substrate," Journal of Crystal Growth, 242, (2002), 270-282 by "Widenborg."

Regarding claim 1, Widenborg discloses a method of forming a polycrystalline semiconductor film on a supporting substrate of foreign material, the method comprising: depositing a metal film onto a target surface of the substrate on which the polycrystalline semiconductor film is to be formed(page 270, column 2, line 10); forming a film of metal oxide and/or metal hydroxide on a surface of the metal(page 271, column 1, lines 1-2); forming a layer of an amorphous semiconductor material over a surface of the metal oxide and/or hydroxide film (page 271, column 1, lines 2-3); heating the substrate, the metal, the metal oxide and/or metal hydroxide film and the amorphous semiconductor material to a temperature at which the semiconductor layer is absorbed into the metal layer and deposited onto the target surface by metal-induced crystallization (MIC) as a polycrystalline layer, whereby the metal is left as an overlayer covering the deposited polycrystalline layer, with semiconductor inclusions in the metal layer, and the polycrystalline semiconductor film and the overlayer separated by a porous interfacial metal oxide and/or metal hydroxide film, with which the semiconductor inclusions are in contact (page 271, column 1, lines 6-8; column 2, lines 1-8); removing the metal in the overlayer and the interfacial metal oxide and/or metal hydroxide film with an etch which under-etches the semiconductor inclusions to form freestanding islands weakly connected to the polycrystalline layer, without significantly thinning the underlying polycrystalline semiconductor layer (page 271, column 2, lines 9-12; page 272, column 1, lines 5-8).

Widenborg appears not to explicitly disclose removing the free standing semiconductor “islands” from the surface of the polycrystalline layer by a lift-off.

Widenborg however discloses that a clean surface with low roughness is beneficial for a seed layer as well as for other potential applications of the poly-Si films (page 271, column 1, lines 12-20).

To obtain the high-quality seed layer therefore it would be obvious "to one of ordinary skill in the art at time the invention was made " [hereinafter not explicitly spelled out in further obviousness rejections, for brevity] to remove the free standing semiconductor "islands" from the surface of the polycrystalline layer by a lift-off.

Regarding claim 4, Widenborg discloses that the substrate comprises a sheet of substrate material over which a preliminary layer is deposited and the target surface is a surface of the preliminary layer (page 271, column 1, section 2, lines 1-10).

As to interpreting scope of claims 6 and 9:

Absent claiming how the intended outcome results are achieved by step limitations, an intended outcome recitation fails to distinguish scope of a method claim over prior art process capable of yielding or achieving the intended outcome language. See, for example, M.P.E.P § 2111.04 and the precedents cited therein

In claim 6 "metal atoms are left in the polycrystalline layer which act as dopants and after the lift-off process, the polycrystalline semiconductor layer is doped with a dopant which overcompensates the doping caused by the metal atoms left in the polycrystalline layer after the MIC step, thereby causing the polycrystalline semiconductor layer to have an overall doping polarity which is opposite to that which would occur due to the metal atoms alone" is intended outcome or intended use, rather than a required step further limiting scope of the claims because the claim recites the a verb tense form different form that used for claim limiting steps. See, for example, M.P.E.P. § 2111.04, and precedents cited therein.

In claim 9 "metal atoms are left in the polycrystalline layer which act as dopants and the amorphous semiconductor material is doped during its formation with atoms that produce an opposite-polarity doping when compared to the polarity of doping caused by the metal atoms left in the polycrystalline layer after the MIC step, the opposite polarity doping being sufficient to overcompensate for the presence of the metal atoms whereby after the MIC step the net doping is opposite in polarity to that which would be produced by the metal atoms alone", is intended outcome or intended use of a required step already disclosed by the prior ar rather than a required

step further limiting scope of the claims because the claim recites the a verb tense form different form that used for claim limiting steps . See, for example, M.P.E.P. § 2111.04, and precedents cited therein.

As to rejecting claims 6 and 9 over the prior art:

Regarding claim 6, Widenborg anticipates the claim because the additional recitations in the claim are intended outcome or use not distinguishing over Widenborg. See above interpretation of scope of the claim and 112(2) rejection.

Regarding claim 9, Widenborg anticipates the claim because the additional recitations in the claim are intended outcome or use not distinguishing over Widenborg. See above interpretation of scope of the claim and 112(2) rejection.

Regarding claim 10, Widenborg discloses that the substrate is a glass (page 271, column 1, section 2, lines 1-3).

Regarding claim 11, Widenborg discloses that the polycrystalline semiconductor film is of a semiconductor material selected from the group comprising silicon (page 271, column 1, section 2, lines 1-3).

Regarding claim 12, Widenborg discloses that the metal is selected such that the metal forms an eutectic solution with the selected semiconductor (abstract discloses Al-Si system).

Regarding claim 21, Widenborg discloses that the metal and metal oxide and/or metal hydroxide etch is performed with a phosphoric acid solution (page 271, column 2, lines 1-9-13).

Regarding claim 22, Widenborg appears not to explicitly disclose that the phosphoric acid solution is a 100% solution of 85% phosphoric acid and etch is performed at 130 ° C +/- 3 ° C for 20 minutes +/- 30 seconds. Widenborg however discloses that the phosphoric acid solution is a 100% solution of 80 % phosphoric acid, and the etch is performed at 55° C for 5 min (page 271, column 2, paragraph 1). The prior art well recognize that parameters of etching (concentration, temperature and time) is critical for the quality of the etching/ cleaning procedure.

According to well established patent law precedent (see, for example, M.P.E.P. § 2144.05) therefore it would have been obvious to optimize (for example by routine experimentations) parameters of etching solution to achieve the optimal cleaning.

Regarding claim 27, Widenborg discloses that the metal layer has a thickness in the range of 30-500 nm (page 271, column 1, section 1, and lines 1-17).

Regarding claim 28, Widenborg discloses that the amorphous semiconductor layer used in the metal-induced crystallization process has a thickness in the range of 30-750 nm (page 271, column 1, section 1, and lines 1-17).

Regarding claim 30, Widenborg discloses that the metal-induced crystallization is performed by annealing the sample at a temperature of 650°C or less (page 271, column 2, lines 1-5).

5. Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over Widenborg as applied to claim 1 above, and further in view of PG Pub 2002/0052096 of an application by "Zhang."

Regarding claim 23, Widenborg discloses all limitations of claim 1 for reasons above. Widenborg appears not to specifically disclose that the lift-off process is selected from the group comprising an acoustic treatment in a solution bath, a brush scrubbing process or a hydrodynamic jet process. Zhang discloses the method of cleaning a silicon substrate by a brush scrubbing process (page 1, [0006]).

To efficiently clean physically adsorbed materials (Zhang, page 1, [0006]) therefore it would have been obvious to use the brush scrubbing process in the lift-off process.

6. Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over Widenborg as applied to claim 1 above, and further in view of "Formation of large-grain uniform poly-Si films on glass at low temperature," Journal of Crystal Growth, 226, (2001), pp. 209-214, by "Aberle."

Regarding claim 25, Widenborg discloses all limitations of claim 1 for reasons above. Widenborg appears not to explicitly disclose that after completion of the lift-off process performing a uniform surface treatment to improve the surface finish of the sample prior to subsequent use of the semiconductor film. Aberle discloses the cleaning treatment of the poly-Si seeding layer before subsequent use of the semiconductor film (page 211, column 1, paragraph 4).

To enhance subsequent epitaxial growth (Aberle, page 211, column 1, paragraph 2) therefore it would have been obvious to one of ordinary skill in the art at time the invention was made to perform a uniform surface treatment to improve the surface finish of the sample prior to subsequent use of the semiconductor film.

7. Claim 32-34, 40, and 50 are rejected under 35 U.S.C. 103(a) as being unpatentable over Widenborg as applied to claim 1 above, and further in view of "Present status of solid phase epitaxy of vacuum-deposited silicon," Journal of Crystal Growth, 98 (1989), pp. 519-530 by "Zotov."

Regarding claim 32, Widenborg discloses all limitations of claim 1 for reasons above. Additionally Widenborg discloses that prepared polycrystalline layer is used as a seed layer for subsequent epitaxial growth (page 270, column 2, lines 6-8).

Widenborg appears not to explicitly disclose cleaning the surface of the seed layer to remove any oxides or other contaminants; forming a second amorphous layer of a semiconductor material over the cleaned surface of the seed layer; heating the substrate, the seed layer and the second amorphous layer to crystallize the semiconductor material by solid phase epitaxy (SPE).

Zotov however discloses and motivates the above limitations.

Specifically, Zotov discloses cleaning the surface of the seed layer to remove any oxides or other contaminants (page 520, column 1, paragraph 2); forming a second amorphous layer of a semiconductor material over the cleaned surface of the seed layer (page 519, column 1, paragraph 2); heating the substrate, the seed layer and the second amorphous layer to crystallize the semiconductor material by solid phase epitaxy (SPE) (page 519, column 1, paragraph 2).

And Zotov explains that performing these steps results in growing silicon films at low temperatures (Zotov, page 528, column 1, section 8, lines 1-5). Zotov additionally notes that such films are used in microwave devices (Zotov, page 519, column 1, and lines 1-3).

To grow silicon films at low temperatures therefore it would have been obvious to perform the above recited steps of claim 32.

Regarding claim 33, in the combination above, Widenborg in view of Zotov discloses that the seed layer and the second amorphous layer are of the same semiconductor material with

the same or different doping (Widenborg, page 271, column 1, lines 16, Zotov, page 519, column 1, last paragraph).

To easing the technological process it would have been obvious to use the seed layer and the second amorphous layers made of the same semiconductor material with the same or different doping.

Regarding claim 34, Zotov discloses that the semiconductor material of the seed layer and the second amorphous layer are different semiconductor materials (page 519, column 2, lines 1-3).

To make heteroepitaxial systems it would have been obvious to use the seed layer and the second amorphous layers made of different semiconductor materials

Regarding claim 40, Zotov discloses that the second amorphous layer is simultaneously doped as it is formed (page 523, column 1, section 5, lines 5-8).

To increase conductivity of the semiconductor material it would have been obvious to use the doped amorphous semiconductor layer.

As to interpreting scope of claim 50

Absent claiming how the intended outcome results are achieved by step limitations, an intended outcome recitation fails to distinguish scope of a method claim over prior art process capable of yielding or achieving the intended outcome language. See, for example, M.P.E.P § 2111.04 and the precedents cited therein.

In claim 50, "amorphous semiconductor material of the second amorphous layer is doped to a predetermined doping profile during an electron beam evaporation deposition process using resistively heated p-type and n-type dopant effusion cells in the vacuum electron-beam evaporation chamber while the deposition process takes place" is an intended outcome or use of a required step already disclosed by the prior art rather than a required step further limiting scope of the claims because the claim recites the a verb tense form different form that used for claim limiting steps. The applied prior art can be so modified or used and therefore renders unpatentable such claims. See, for example, M.P.E.P. § 2111.04, and precedents cited therein.

As to rejecting claim 50 over the prior art:

Regarding claim 50, Zotov anticipates the claim because the additional recitations in the claim are intended outcome or use not distinguishing over Zotov. See above interpretation of scope of the claim and 112(2) rejection.

8. Claim 54 is rejected under 35 U.S.C. 103(a) as being unpatentable over Widenborg in view of Zotov, and further in view of US Patent 6,620,743 to "Pagliaro."

As to interpreting scope of claims 54:

Absent claiming how the intended outcome results are achieved by step limitations, an intended outcome recitation fails to distinguish scope of a method claim over prior art process capable of yielding or achieving the intended outcome language. See, for example, M.P.E.P § 2111.04 and the precedents cited therein.

In claim 54, " the substrate is transferred to the semiconductor deposition chamber within 60 minutes of completion of the cleaning step" is an intended outcome or use of a required step already disclosed by the prior art rather than a required step further limiting scope of the claims because the claim recites the a verb tense form different form that used for claim limiting steps. The applied prior art can be so modified or used and therefore renders unpatentable such claims. See, for example, M.P.E.P. § 2111.04, and precedents cited therein.

As to rejecting claim 54 over the prior art:

Regarding claim 54, Widenborg in view of Zotov discloses all limitations of claim 32 for reasons above. Additionally, in the above combination Zotov discloses that the substrate is transferred to the semiconductor deposition chamber after the cleaning step (page 520, column 1, paragraph 3). Widenborg in view of Zotov appears not to explicitly disclose that the step of cleaning the seed layer surface comprises a process which creates a hydrogen-terminated silicon surface. Pagliaro discloses the cleaning method that leads to a hydrogen-terminated silicon surface (abstract).

To obtain oxide-free stable silicon surface therefore it would have been obvious to use the process which creates a hydrogen-terminated silicon surface.

CONCLUSION

9. A shortened statutory period for reply to this Office Action is set to expire **THREE MONTHS** from the mailing date of this Office Action. Applicant is reminded of the extension of time policy as set forth in 37 CFR § 1.136(a).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JULIA SLUTSKER whose telephone number is (571)270-3849. The examiner can normally be reached on Monday-Friday, 8 a.m.-5 p.m. EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, William Baumeister can be reached on (571)-272-1722. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JS
/HRAYR A. SAYADIAN/
Primary Examiner, Art Unit 2815